

10. Integrated circuit according to claim 1, characterized in that it comprises means (Pd, C2) for extracting a d.c. supply voltage (Vcc) from the a.c. voltage (Vac) induced in the antenna coil (Ls).

11. Integrated circuit according to claim 1, wherein the means for inhibiting the clock extraction device (CEC1) comprises means (T5, T6) for powering-off the extraction device (CEC1).

IN THE ABSTRACT

Please add page 22 containing an Abstract of the Disclosure.

REMARKS

The application has been amended to insert headings in the specification, to eliminate the multiple dependencies in the claims, and to add an Abstract of the Disclosure.

Entry of the amendments and examination of the continuation international application are respectfully requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

3. (Amended) Integrated circuit according to [one of the claims 1 and 2] claim 1, wherein the means (CC1) for delivering the pulsed modulation signal (S_{lm4}) comprise at least two capacitors (C_{ref}, C_{as}) and means (WLCC, CG1, CMP, D6, SR1, T1, T2, T3, T4) for:

- charging the first capacitor (C_{ref}) with a constant current (I_{ref}) before the emission of a load modulation pulse, during a time (T_{ref}) fixed by a predetermined number of clock cycles (H),
- charging the second capacitor (C_{as}) with a constant current (I_{ref}) during the emission of a pulse, and
- stopping the emission of the pulse when the charge voltage (V_{as}) of the second capacitor is equal to the voltage (V_{ref}) at the terminals of the first capacitor.

4. (Amended) Integrated circuit according to [one of the claims 1 to 3] claim 1, comprising means (WLCC) for:

- transforming the binary signal to be transmitted (DT_x) into a binary coded signal (S1) presenting at least, at each bit of the binary signal, a rising or falling variation edge, and
- transforming variation edges of the binary coded signal (S1) into load modulation pulses (I_l-I_n) of short duration compared to the duration (T_b) of a bit of the binary signal to be transmitted (DT_x).

6. Integrated circuit according to [one of the claims 1 to 5] claim 1, wherein the modulation signal (S_{lm4}) is combined with an a.c. signal (F_{sc}) in order to form a load modulation signal comprising a.c. signal pulses.

7. Integrated circuit according to [one of the claims 1 to 6] claim 1, wherein the load modulation pulses have a duration (T_{as}) shorter than or equal to the quarter of the duration of a bit of the binary signal to be transmitted (DT_x).

8. Integrated circuit according to [one of the claims 1 to 7] claim 1, wherein the clock extraction device (CEC1) is maintained in an inhibited state after the emission a load modulation pulse, at least for a time (T_{ref} , T_{as}) equal to the duration of a load modulation pulse.

9. Integrated Circuit according to [one of the claims 1 to 8] claim 1, wherein the clock extraction device (CEC1) is arranged to extract a clock signal (H) from an a.c. voltage (V_{ac}) induced in the antenna coil (L_s).

10. Integrated circuit according to [one of the claims 1 to 9] claim 1, characterized in that it comprises means (P_d , C_2) for extracting a d.c. supply voltage (V_{cc}) from the a.c. voltage (V_{ac}) induced in the antenna coil (L_s).

11. Integrated circuit according to [one of the claims 1 to 10] claim 1, wherein the means for inhibiting the clock extraction device (CEC1) comprises means (T_5 , T_6) for powering-off the extraction device (CEC1).

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